ABSTRACT

Large, complex SoCs comprise interconnections of various functional blocks, which blocks frequently running on different clock domains. By effectively controlling the clocks within the SoC, this invention provides a means to halt execution of a SoC and to then single or n-cycle step its execution in a real system environment. Accordingly, the invention provides an effective debugging tool to both the SoC designer and software designers whose code is executed by the SoC as it provides them the capability of studying the cause and effect of interactions between functional blocks. The invention is also applicable to SoCs containing only one functional block while containing complex circuitry operating on a clock different than the block's clock. In particular, the invention permits halting of the block clock and then single or n-cycle stepping its execution to permit analysis of the interactions between the block and the SoC circuitry.